Abstract

A network processor or other type of processor includes in an illustrative embodiment a first pass classifier coupled to first memory circuitry in the form of a relatively small internal memory, and a second pass classifier coupled to second memory circuitry in the form of a larger internal buffer memory. The first memory circuitry is configurable to store at least a portion of a given packet to be processed by the first pass classifier. The second memory circuitry is configurable to store a different and preferably smaller portion of the given packet to permit processing thereof by the second pass classifier. The portion of the given packet storable in the second memory circuitry is a portion of the given packet determined by a first pass classification, performed by the first pass classifier, to be required for a second pass classification, performed by the second pass classifier. Advantageously, the invention reduces the size of the packet portion required to be stored in the second memory circuitry, thereby reducing the required memory of the processor. The processor may be configured as a network processor integrated circuit to provide an interface between a network from which the packet is received and a switch fabric in a router or switch.